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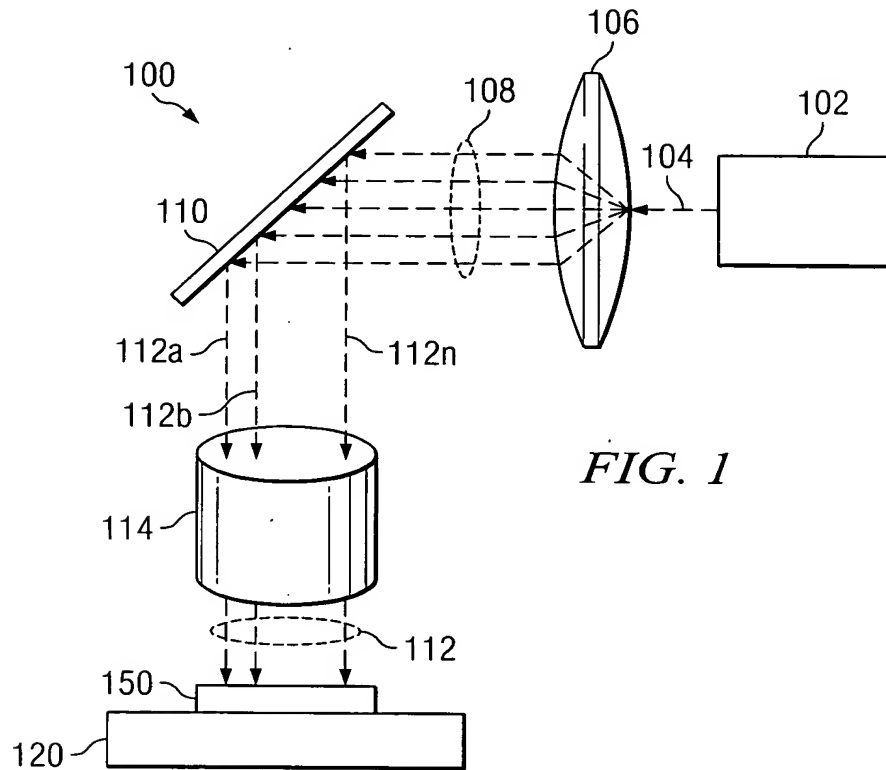


FIG. 1

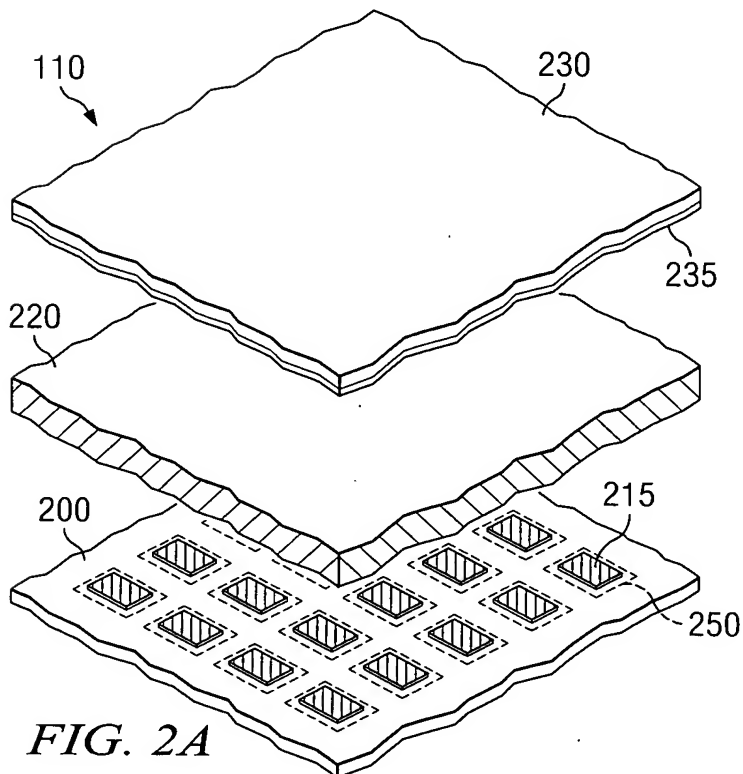


FIG. 2A

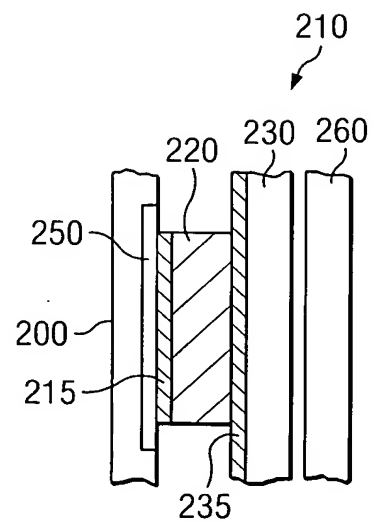
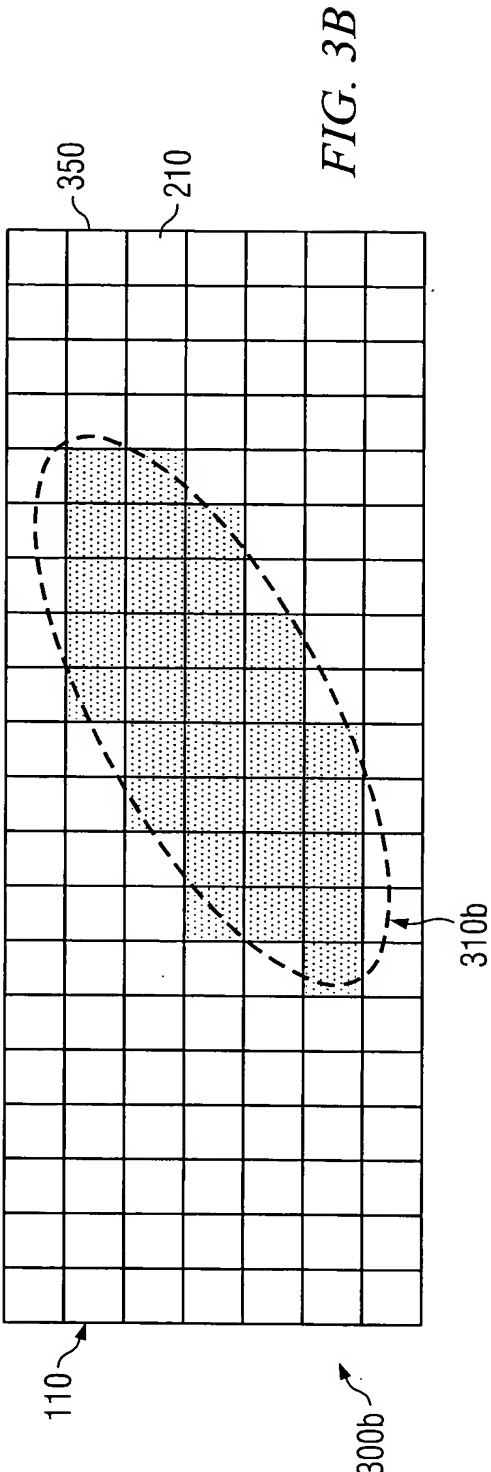
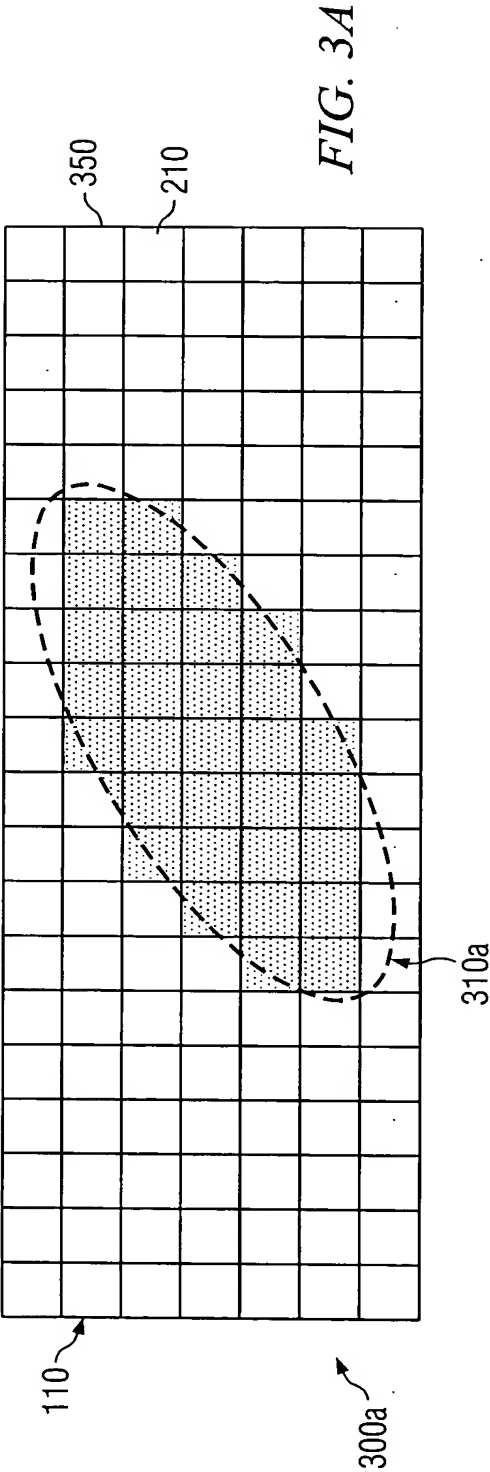
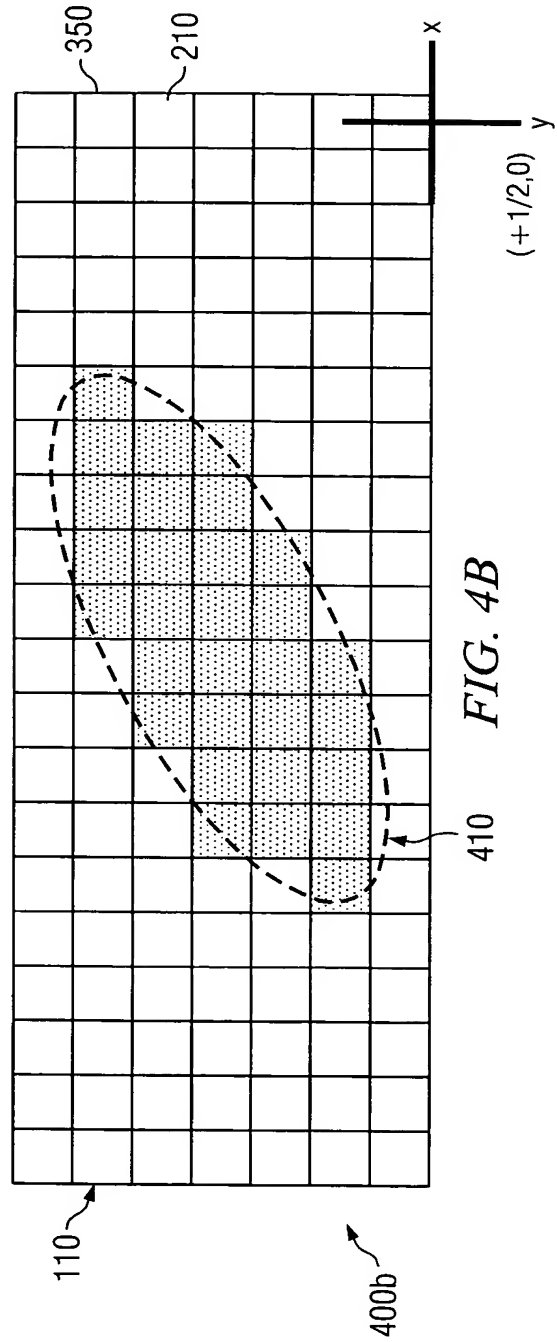
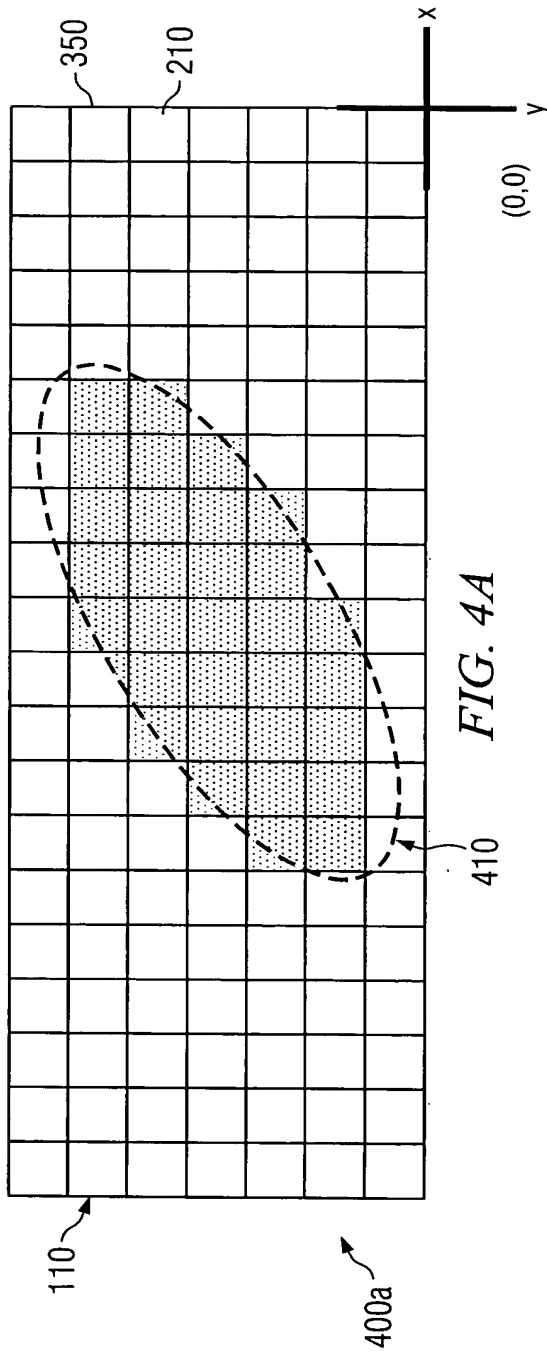
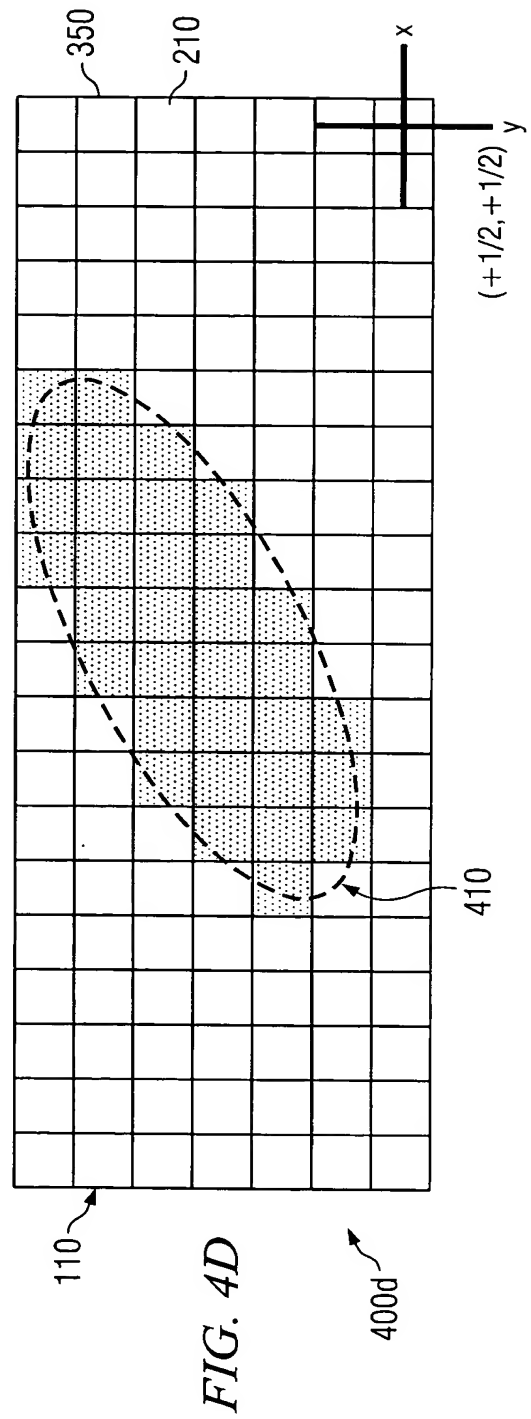
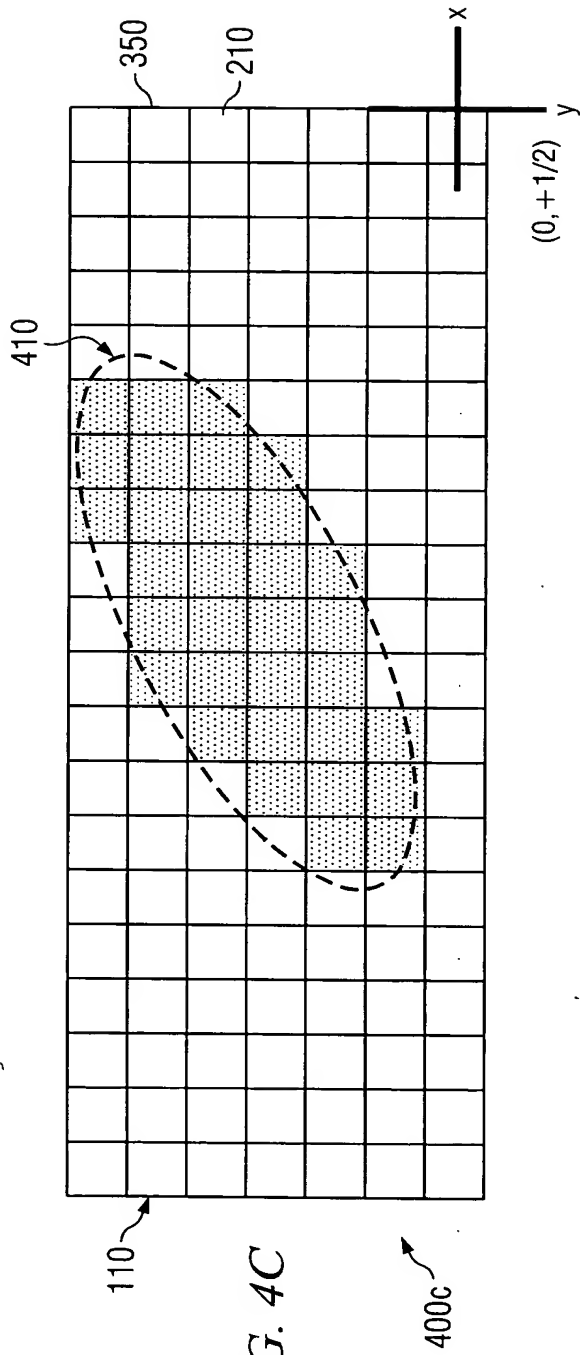
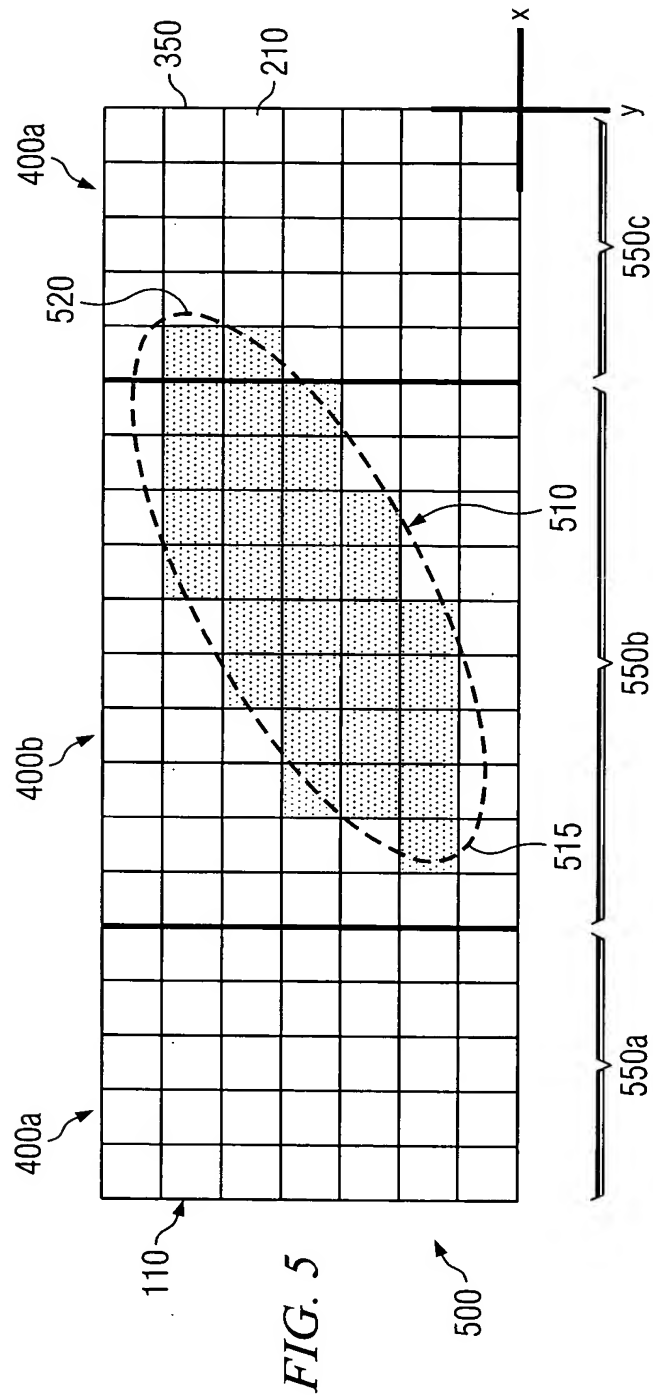


FIG. 2B









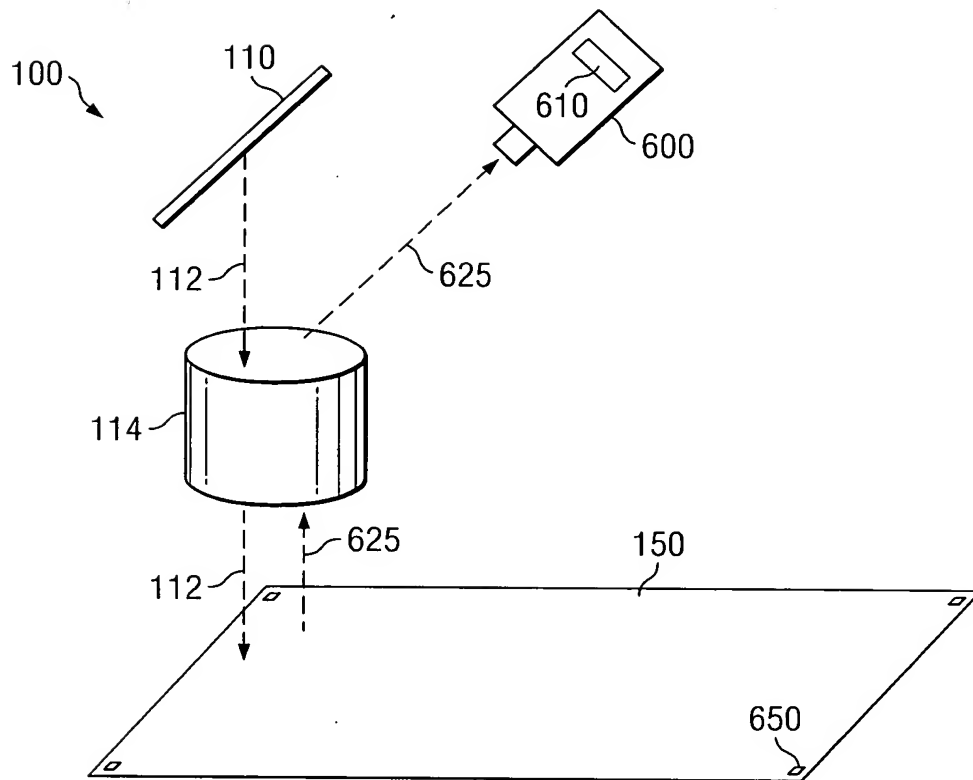


FIG. 6

Diagram of a display device 700. The device includes a display panel 760 and a display area 500.



The diagram illustrates a misalignment correction system. It features four input blocks, labeled 400a, 400b, 400c, and 400d, each containing four sub-blocks labeled 425a, 425b, 425c, and 425d. These input blocks are connected to a central processor (710). The processor also receives distortion information (735) and a misalignment threshold (780). The processor outputs to a block (500) containing four sub-blocks labeled 550a, 550b, 550c, and 550d, which then produces the final output (OUT).

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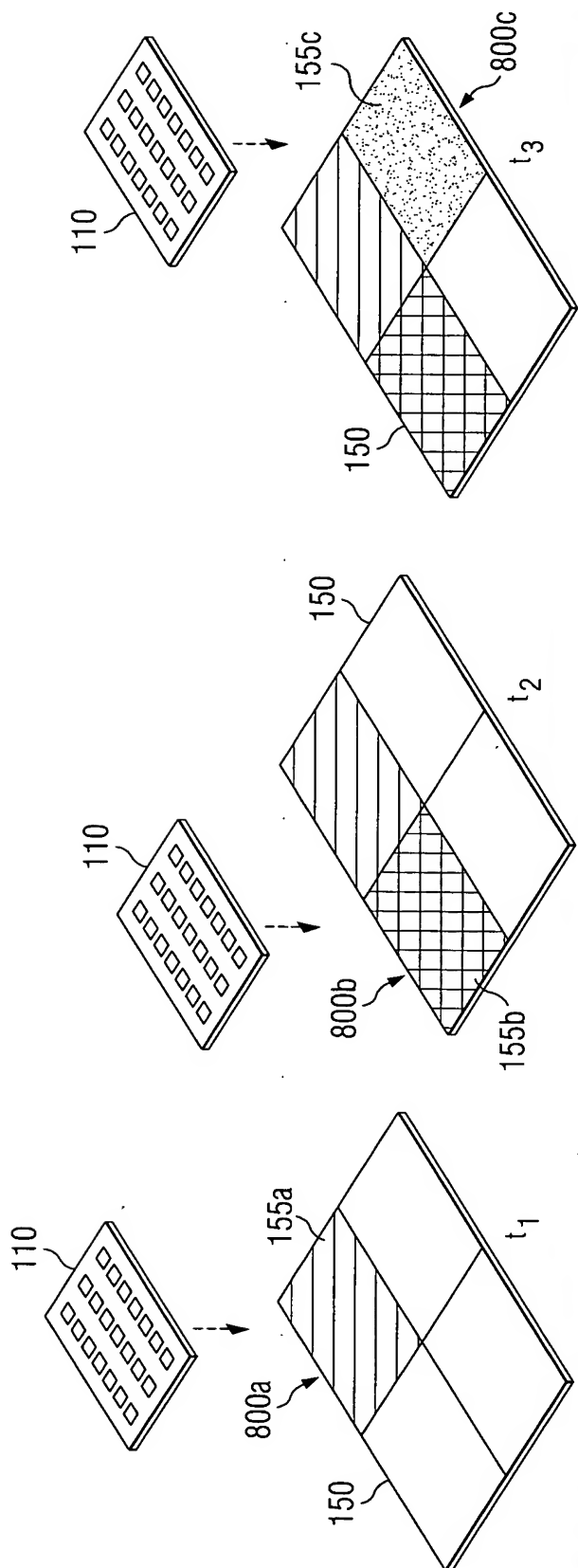


FIG. 8



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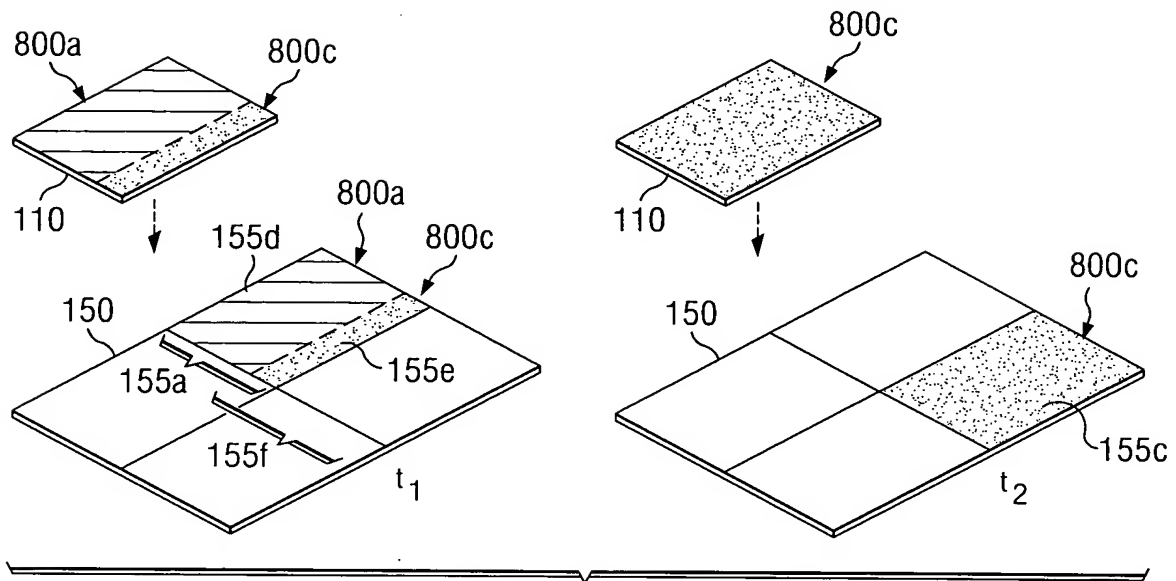


FIG. 9A

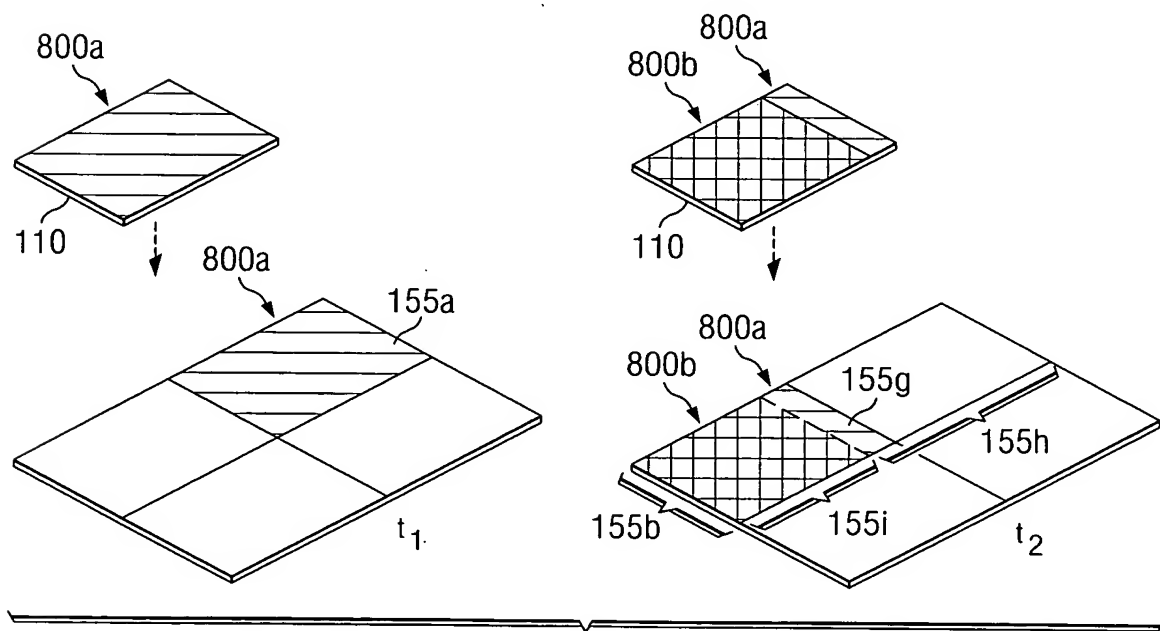


FIG. 9B

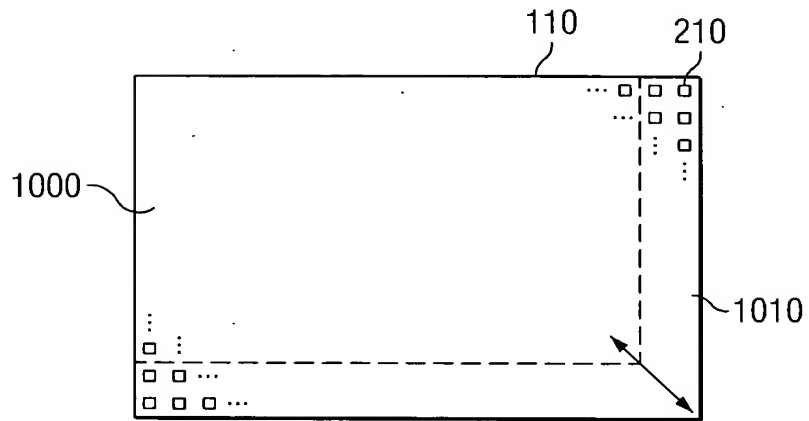


FIG. 10

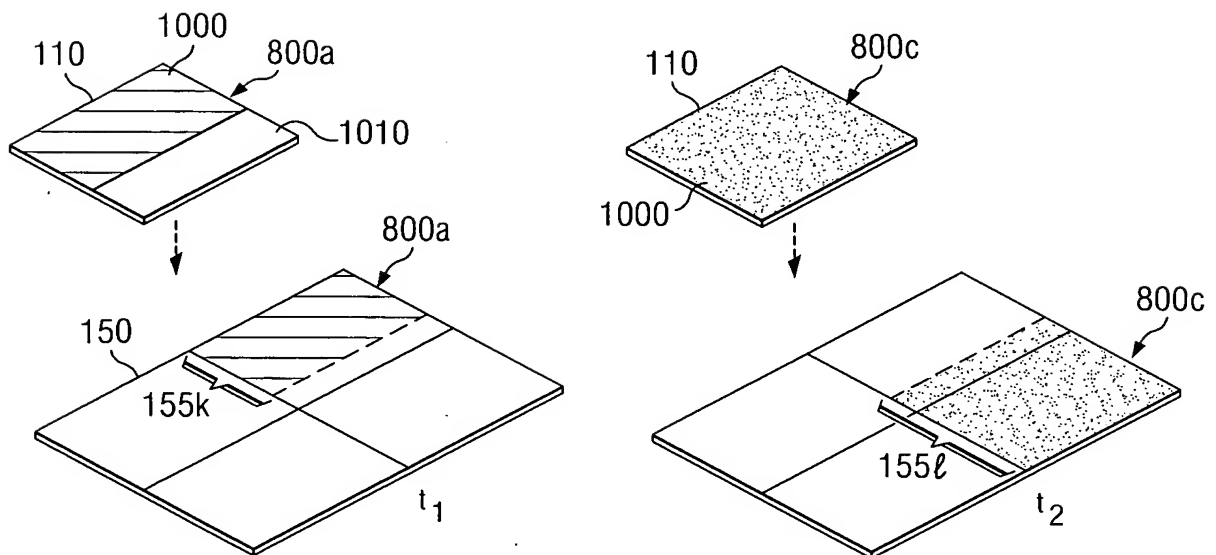


FIG. 11

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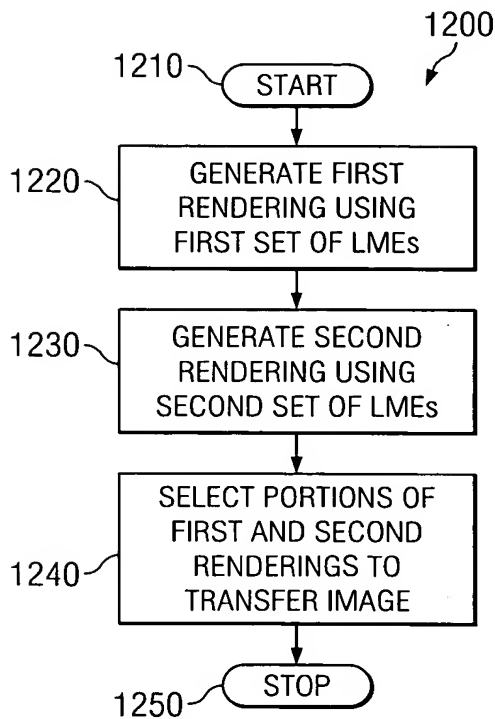


FIG. 12

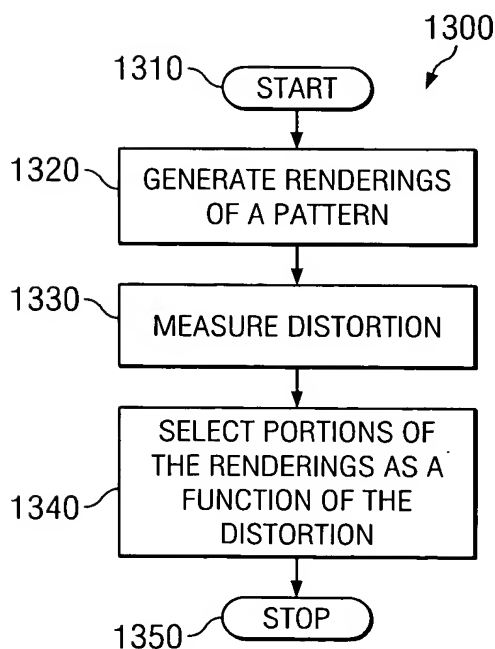


FIG. 13

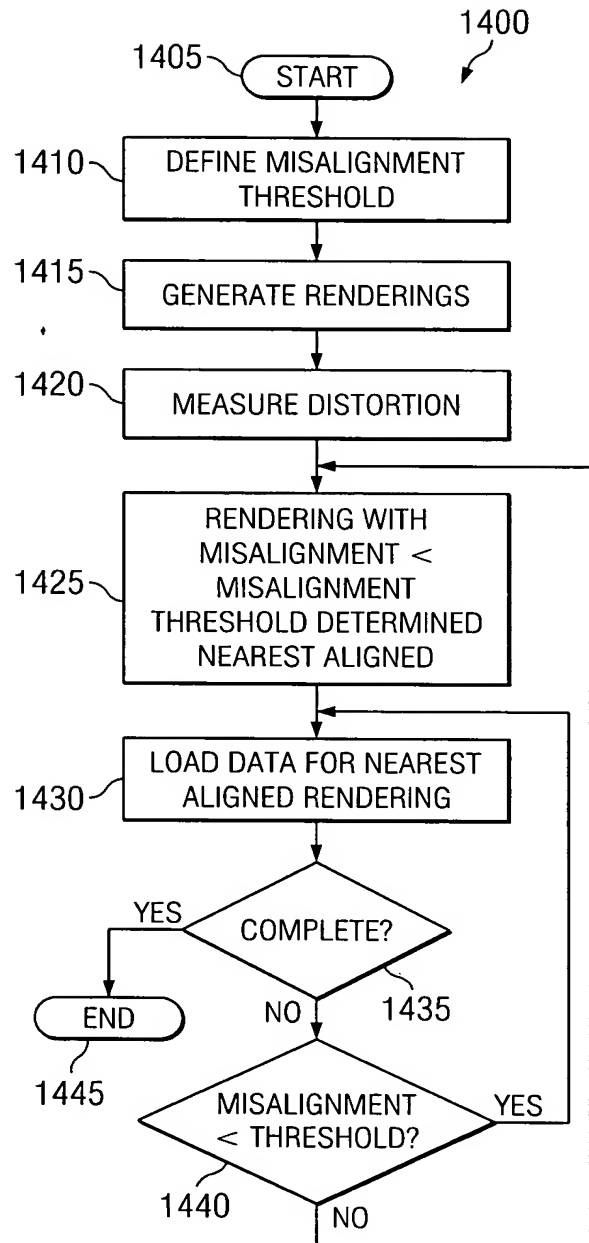


FIG. 14

